HIGH SCHOOL EDITION
Journal of Student Research
Volume 13 Issue 3 (2024)

Cu-Cu Bonding of 3DIC

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ABSTRACT

This paper presents study on the manufacturing process of Cu-Cu direct bonding for 3DIC. Main procedures include RCA cleaning, SiO_2 film growth, lithography, E-gun deposition, adhesion layer deposition, cleaning and Cu oxide layer removal, dicing, and bonding. Of the two cleaning methods—plasma treatment and acid treatment—employed on wafers, the one with plasma treatment demonstrate superior bonding strength. The study results encompass SEM, pull tests, SAT, and TEM examination results on bonding condition of wafer with both plasma and acid treatment. This research offers insights into optimizing the fabrication process for enhanced performance in Cu-Cu direct bonding for 3DIC applications.

Motivation

With increasing demands for high-performance chips – chips that come in reduced sizes and additional features at a lower cost, to operate precision apparatus, we tend to develop smaller chips but expect higher performance in the meantime. However, when it comes to nano-meter scale, the high density of interconnection in IC causes lagging, which is a severe disruption to the whole procedure. To solve this problem, scientists developed a brand-new technique—3DIC. The advantages of 3DIC include smaller sizes, lower energy consumption, shorter wires between electronic components, lower cost, and multiple functions. To understand more about how Cu-Cu Bonding on 3DIC works, we want to go through the process and examine different features of the bonding.

Method

Process Flow

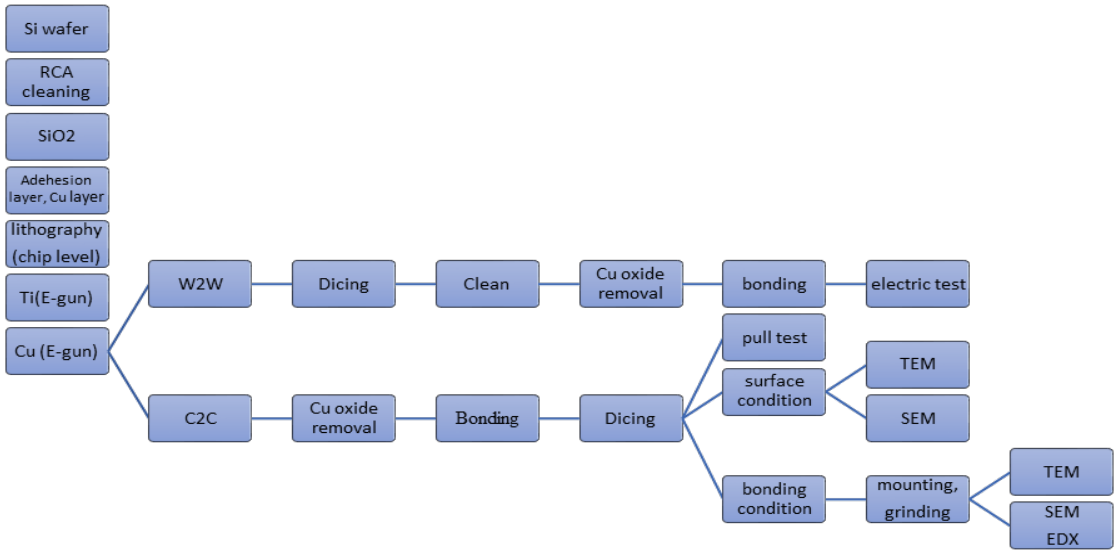

Figure 1. Process flow

RCA (Radio Corporation of America)

- RCA is a cleaning process commonly associated with a pivotal semiconductor wafer utilized in the electronics industry. The procedure involves two main steps: SC-1 (Standard Clean-1) and SC-2 (Standard Clean-2). In SC-1, a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and water (H_2O) in a ratio of 1:4:5 is prepared, heated to a temperature ranging from 75 to 85 degrees Celsius, and applied to silicon wafers for a duration of 10 to 20 minutes. SC-2 follows a similar protocol, with a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2), and water (H_2O) in a ratio of 1:1:6, also heated to 75 to 85 degrees Celsius and applied for 10 to 20 minutes. These rigorous cleaning processes are vital for removing organic contaminants from the surface of the wafers, ensuring the quality and integrity of semiconductor materials used in electronic device manufacturing. Next, deionized water will be used to remove residual solution on the wafer. Finally, the surface will be dried.

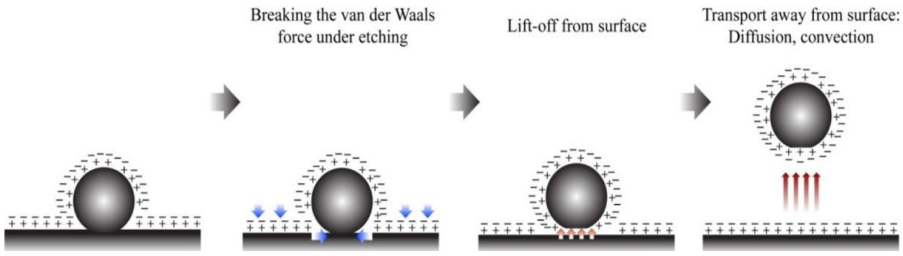

Figure 2. RCA cleaning

SiO_2 Film Grow

Silicon dioxide (SiO2) film growth is a crucial process in semiconductor fabrication, particularly for forming isolating layers that prevent electronic components from interfering with each other. This isolation is essential for ensuring the proper functioning and reliability of electronic devices. The method we use for growing SiO2

films is through the wet oxidation process, often conducted in a furnace environment. During wet oxidation, a mixture of hydrogen (H_2) and oxygen (O_2) gases is introduced into the furnace chamber, where it reacts with silicon substrates. The reaction between silicon and water vapor (H_2O) leads to the formation of silicon dioxide according to the equation: $Si + H_2O \rightarrow SiO_2$, with silicon film being consumed in the process. This method allows for controlled growth of SiO_2 layers on silicon substrates, providing the necessary insulation for electronic components and contributing to the overall functionality and performance of semiconductor devices.

Lithography (Chip Level Specifically)

Lithography is a pivotal process in semiconductor manufacturing, essential for patterning structures onto silicon wafers. The procedure encompasses several sequential steps to achieve precise patterning. It begins with the application of a photoresist (PR) coating onto the silicon wafer, forming a light-sensitive layer. Following this, the wafer undergoes exposure to UV light through a photomask containing the desired pattern, inducing chemical changes in the photoresist layer. The subsequent development step involves immersing the exposed wafer in a developer solution, selectively removing the exposed (positive photoresist) regions, revealing the desired pattern. Then, metal deposition occurs, where a thin layer of metal is deposited onto the wafer surface, conforming to the pattern defined by the photoresist. Finally, the remaining photoresist is removed by ACE, leaving behind the patterned metal features on the wafer surface.

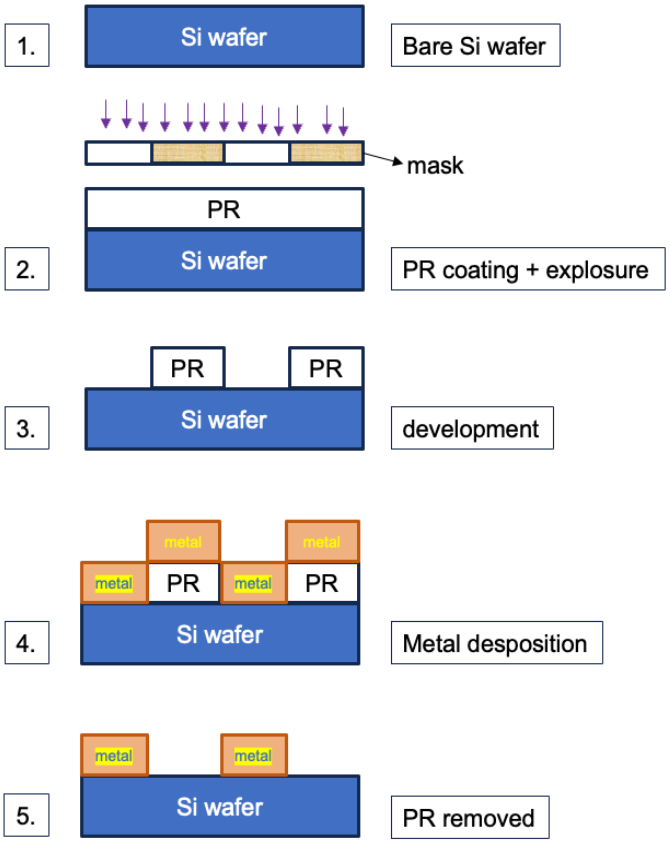

Figure 3. Process of lithography

E-Gun

E-gun machine uses electron beam to heat the target material to its melting temperature, causing it to melt and vaporize. At this point, the molecules of the thin film material in the gaseous state, which have acquired kinetic energy from the heating, fly toward the substrate, arriving and adhering to the surface of the substrate.

Figure 4, Figure 5. E-gun

Adhesion Layer and Copper Layer Deposition

The aim of the procedure is to deposit a layer of copper (Cu) onto the wafer surface using evaporation techniques. To achieve this, we employ a method known as Ti/Cu deposition utilizing an electron beam gun (E-gun) within the framework of Physical Vapor Deposition (PVD). This process involves initially depositing a thin layer of titanium (Ti) with a thickness of 30nm onto the wafer surface. The role of the Ti layer is to enhance adhesion between the subsequent copper layer and the underlying substrate. Following the Ti deposition, a thicker layer of copper, approximately 300 nm in thickness, is then evaporated onto the wafer surface using the same E-gun technique. By employing this Ti/Cu deposition approach with evaporation, our objective is to ensure efficient deposition of the copper layer onto the wafer while also promoting strong adhesion between layers. This method enables us to effectively integrate copper into our semiconductor device fabrication process, contributing to the overall performance and functionality of the final product.

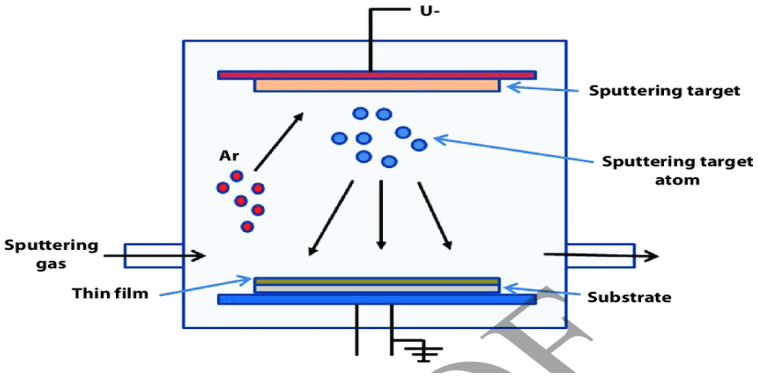

Figure 6. PVD

Cleaning and Cu Oxide Layer Removal (Employing Two Different Methods)

Acid

To clean and remove the copper oxide layer, a solution of 5% sulfuric acid is used to wash out the oxide. After the acid treatment, the surface is thoroughly rinsed with deionized (DI) water. This process ensures that no residue is left on the chip. Additionally, X-ray photoelectron spectroscopy (XPS) can be employed to confirm the absence of any remaining contaminants.

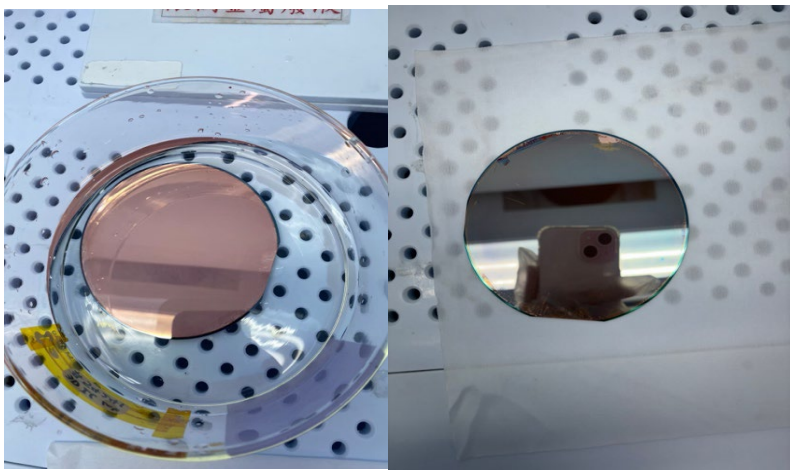

Figure 7, Figure 8. Acid

Plasma

Another cleaning method is plasma bombardment. Plasma is employed to remove copper oxide from the surface. This process is carried out at two levels: wafer level and chip level. At wafer level, argon gas is used at 250W for 4 minutes, while at the chip level, argon gas is applied at 100W for 3 minutes. This technique effectively eliminates the copper oxide, ensuring a clean and prepared surface for further processing or analysis.

Figure 9, Figure 10. Plasma

Bonding (Thermal Compression Bonding)

Thermal compression bonding, also known as TCB, is a process that involves heating and applying both thermal and mechanical pressure to fuse two bodies together. This method is utilized under specific conditions, differentiated between wafer level and chip level applications. At the wafer level, a force of 10 kN is applied at 300 °C for 50 minutes. On the other hand, at the chip level, a force of 200 N is applied at the same temperature of 300 °C but for a shorter duration of 3 minutes. These conditions ensure proper bonding between the materials, facilitating reliable and durable connections in electronic or microfabrication processes.

Figure 11. Bonding wafer level

Dicing (Wafer to Wafer)

Dice the wafer into several smaller units.

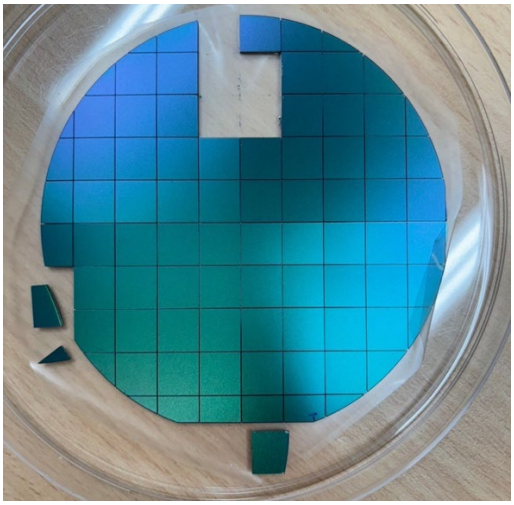

Figure 12. Dicing

Bonding Interface Treatment for Further Examination

Mounting

Mounting is a crucial step that involves securing the chip with a butterfly clip in an upright position. This setup is essential for enabling the observation of the cross-section of the bonding interface using subsequent instruments. Additionally, the ratio of Colophony to Hardener is maintained at 16:5, emphasizing the precise mixture required for the bonding process.

Figure 13, Figure 14. Mounting and solidification

Grinding and Polishing interface

By grinding and polishing interface process, we can improve the quality and performance of the wafter by reducing its surface roughness and removing any defects on contamination.

Results and Discussion

SEM

Plasma

This is the bonding interface of wafer employed by plasma treatment under SEM (with bonding interface)

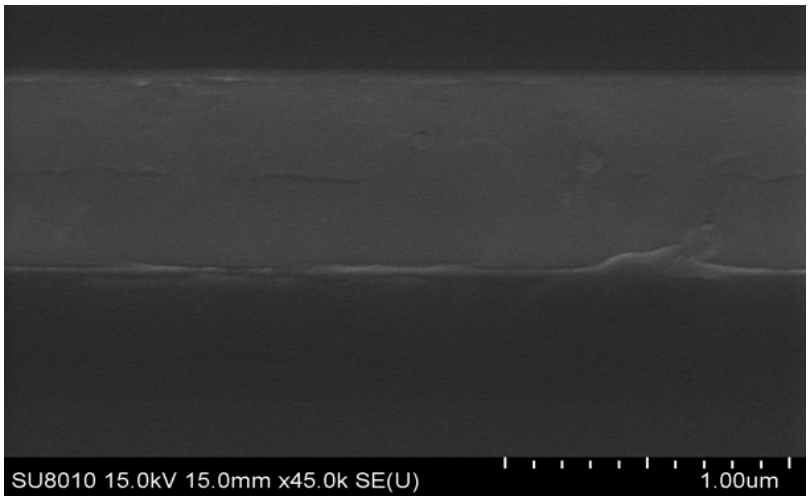

Figure 15. Plasma- bonding interface under SEM

Acid

This is the bonding interface of wafer employed by acid treatment under SEM, and the granular appearance on the surface may be caused by grinding or incomplete bonding.

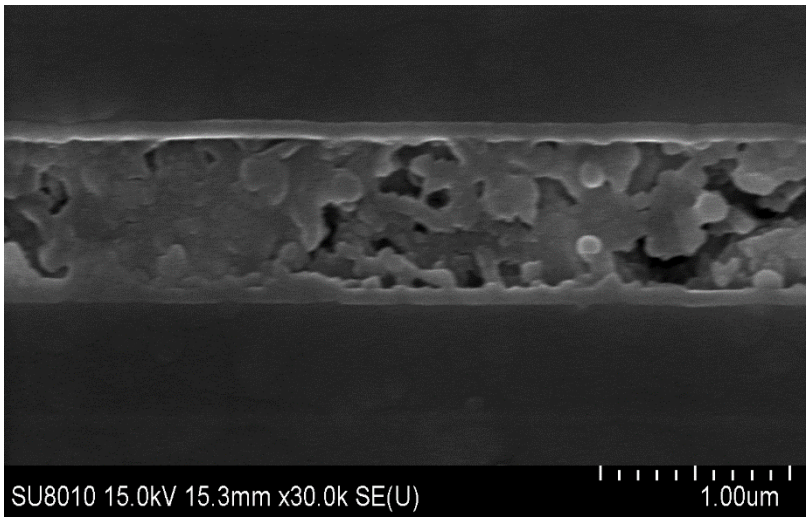

Figure 16. Acid-bonding interface under SEM

Pull Test

This diagram represents the deformation-load capacity relationship of two samples cleaned separately with plasma and acid in a pull test.

Table 1. Bonding strength by pull test.

	plasma (MPa)	acid (MPa)
sample 1	13.3096	9.6285

sample 2	9.6907	8.6024
average	11.5002	9.11545

The figure below shows that wafers treated with plasma have better bonding strength in mechanical tests compared to those treated with acid. Discussing the average data of the two groups, the bonding strength of plasma is 11.5 MPa, while that of acid is approximately 9.12 MPa. The reason for the higher strength after plasma treatment is speculated to be due to the more effective removal of copper oxide layers by plasma.

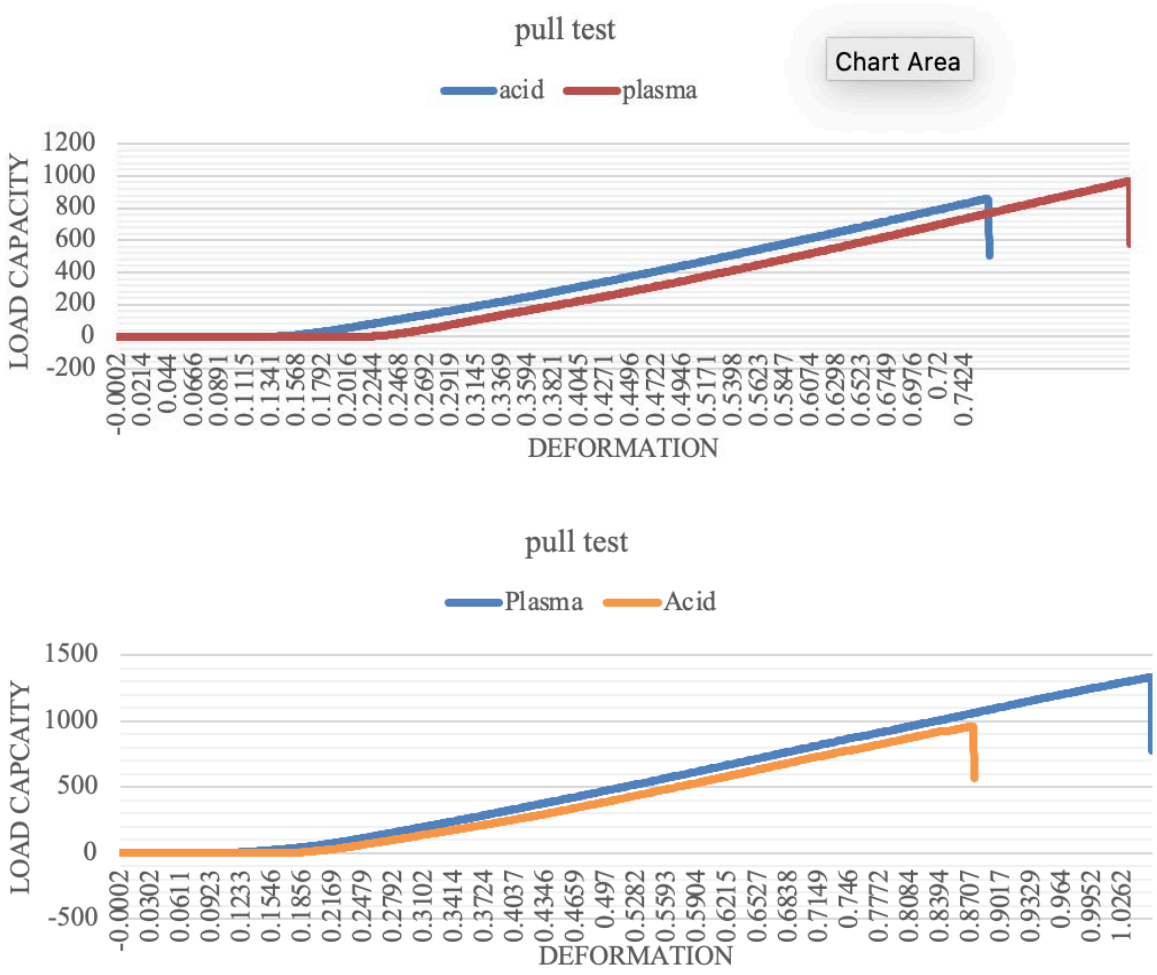

Figure 17, Figure 18. Pull test results.

SAT (Scholastic Assessment Test)

The two figures show the bonding status of two different wafers under SAT followed by treatment with plasma and acid, respectively. The black areas represent well-bonded regions, while the white areas may indicate holes or particles. On the right side, there is a large area of misalignment due to improper alignment during bonding.

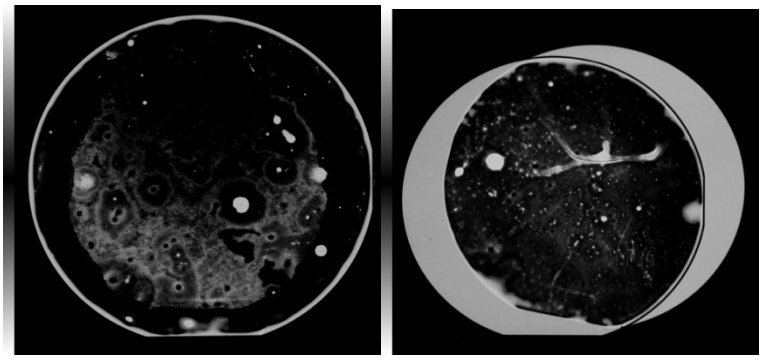

Figure 19, Figure 20. SAT results

TEM (Transition Electron Telescope)

Figures 21, 22 (wafer employed with plasma treatment) and Figures 24, 25 (wafer employed with acid treatment) show the bonding interface at a low magnification under TEM. The white areas in the images represent gaps at the bonding interface. The gaps occur because the interface is formed by combining two separate parts, rather than being a continuous piece of metal. This means the connection at the interface is relatively weak. Hence, when the sample is hit by the high-energy electron beam of a TEM or the high-energy ion beam of an FIB, the weaker bonding interface may be damaged, causing the gaps to appear.

Figures 23 and 26 show the bonding interface at a magnification of 800k under TEM. By comparing the thickness of the transition layer (where the atomic arrangement is less orderly) near the bonding interface, we can presume whether the wafer with plasma treatment or acid treatment has better bonding condition. However, to ensure the actual bonding strength, we still must employ mechanical tests, such as pull tests, to determine which one has stronger bonding strength.

Figures 24 and 27 are FFT (also known as diffraction pattern or DP) images. By examining the positions of the points, we can determine metal's crystallization condition. The disordered areas indicate where the bonding interface is.

Plasma

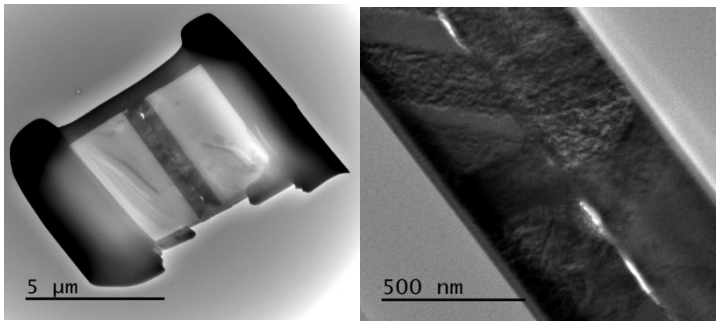

Figure 21, Figure 22.

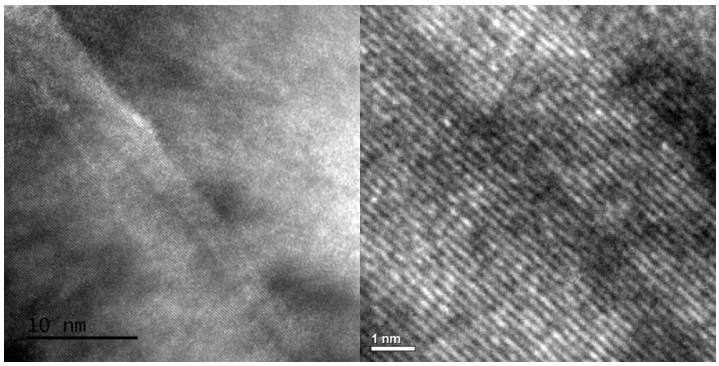

Figure 23, Figure 24.

Acid

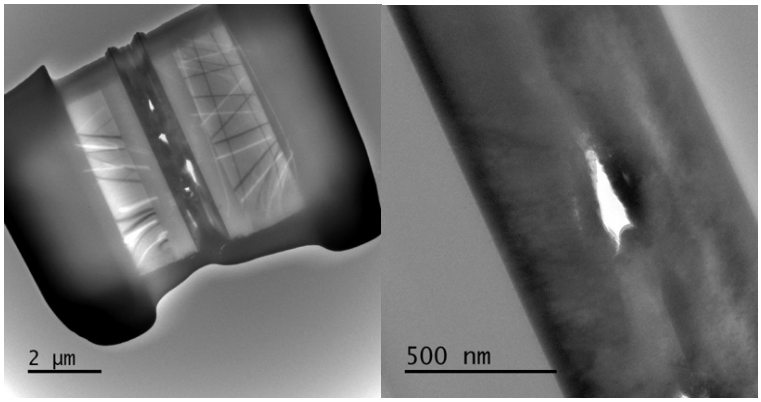

Figure 24, Figure 25.

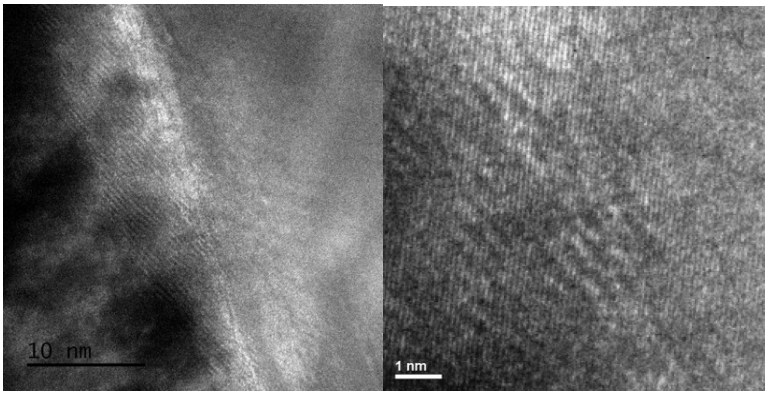

Figure 26, Figure 27.

Electrical Tests

Due to the high power of the plasma machine, it damaged the circuit (as shown in the left image), resulting in higher resistance values for the wafer treated with plasma. Therefore, it is difficult to compare the advantages and disadvantages of the two based on electrical test results.

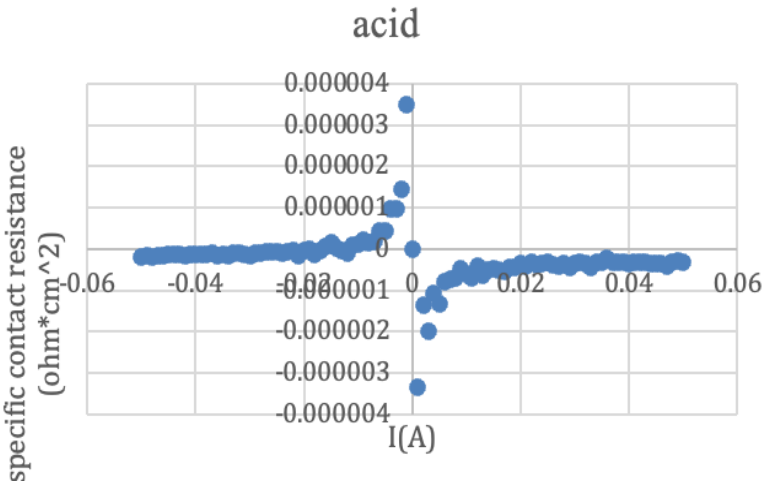

Figure 28. Electrical test (acid)

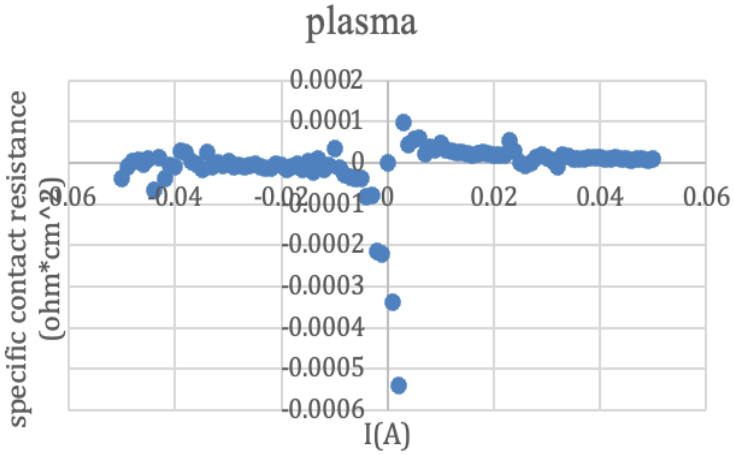

Figure 29. Electrical test (plasma)

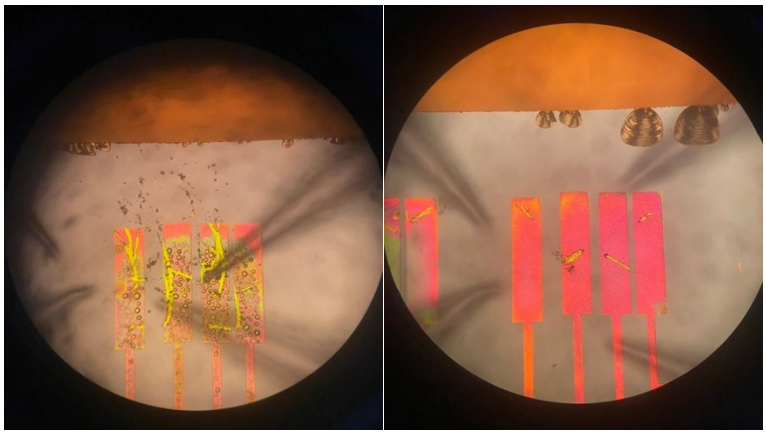

Figure 30, Figure 31. Electrical tests

Acknowledgments

I would like to thank my advisor for the valuable insight provided to me on this topic.

References

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/*PVD*/*CVD*: https://www.sciencedirect.com/topics/materials-science/chemical-vapor-deposition#:~:text=The%20CVD%20process%20involves%20depositing,the%20materials%20to%20be%20coated.

Figure

/*PVD*: TRIBOLOGY AND CHARACTERIZATION OF SURFACE COATINGS Edited by Sarfraj Ahmed and Vinayak S. Dakre Copyright: 2021 ISBN: 9781119818786 - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Schematic-diagram-of-the-physical-vapor-deposition-PVD_fig2_357734945 [accessed 3 Jan, 2024]

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