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Investigating The Performance and Viability of Semiconducting Graphene as A Substitute for Silicon in Field Effect Transistors

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ABSTRACT

This paper investigates the electrical and thermal properties of two competing methods of semiconducting graphene, doped graphene and reduced graphene oxide, and their respective viabilities for implementation in field effect transistors. We used the Graphene Field Effect Transistor (GFET) simulation software on nanohub.com to determine the current, voltage, and max temperature based on variations in the channel length, top gate oxide thickness, electron mobility, and thermal conductivity and then compared these performance results with those of a traditional silicon-based transistor. Our results demonstrated that doped graphene had superior current conductivity, higher electron mobility, higher thermal conductivity, and higher maximum temperature to those of reduced graphene oxide and silicon. Practicality wise, reduced graphene oxide is far easier to mass produce, as was found to still perform better than silicon-based transistors. Transistors form the backbone of the electronics industry; this study proves that a shift toward graphene-based transistors, doped ones especially, would make transistors stronger, more durable, and more efficient. With the already ubiquitous usage of transistors in our everyday lives, a switch to graphene could bring revolutionary benefits for electronics such as smarter cell phones, faster computers, and more accurate biosensors.

Introduction

From architecture to electronics to energy, materials play an undeniably important role in our everyday lives. With constant research and testing of new materials, scientists have noticed materials with extreme mechanical, optical, thermal, or electrical properties such as very strong nanocomposites or highly conductive semiconductors. Not only are these scientists trying to generate materials with superior properties, but also materials that can be applied in a variety of different fields. In recent years, scientists have finally found the perfect material that meets both criteria, has a wide variety of applicable fields and is promised to revolutionize the materials industry: graphene. Graphene—a two-dimensional allotrope of carbon with a hexagonal crystalline structure—has been gaining enormous popularity, with some scientists even dubbing it a “miracle material”. This is because graphene exhibits many highly favorable properties including an “extremely high thermal conductivity, excellent electrical conductivity, a high surface-to-volume ratio, remarkable mechanical strength, and biocompatibility” [1]. As one of the most conductive materials on the planet, pure graphene has an electron mobility of 200,000 cm2/(V·s) and a thermal conductivity of 5000 W/mK. While pure graphene does possess extraordinary material properties, graphene is very rarely utilized in the electronics industry. One of the main issues of pure graphene usage is the difficult process of synthesizing it, a problem as old as scientists have known about it. There currently lacks a standardized, efficient, way to mass produce pure graphene for use in industry. Another problem with graphene usage as it stands is quantity. Because graphene itself is only an atom thick, it will not only be very difficult but also hugely time-consuming to produce a lot of it. A third problem lies in the very nature of graphene itself: it isn’t a semiconductor. Pure graphene is classified as a semimetal, meaning it lacks the band gap in its band structure necessary to be a viable material for electronics.

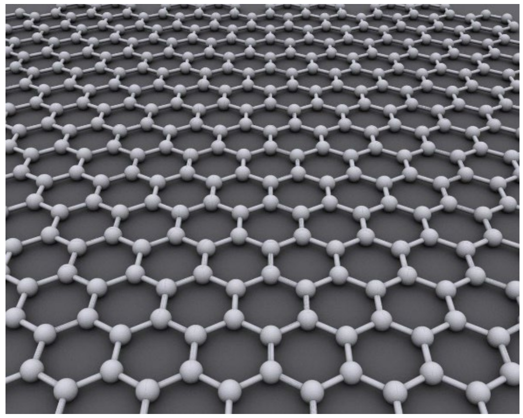

Figure 1. Crystalline lattice molecular structure of pure graphene

However, there are methods that can turn graphene into a semiconductor, of which this research paper will specifically focus on two of: doping and reduced nanocomposites. Furthermore, this paper will investigate the performance results when these so-called graphene semiconductors are applied to field effect transistors (FETs), especially when compared to the traditional silicon-based ones. These transistors, which are commonly used in amplification devices, work by using the voltage applied to its gate to control current running from its source terminal to its drain terminal. Traditionally, silicon nanowires were the most popular materials used in these transistors because of their semiconducting properties and abundance in industry. Recently, however, scientists have discovered that when graphene is doped, or combined with oxygen, it produces modified materials with enlarged band gaps, essentially turning graphene into a semiconductor that is immensely stronger than silicon. Furthermore, both methods are much easier and more efficient to produce than pure graphene. Both graphene oxide and graphene doping are on the rise to becoming potentially viable strategies to replace silicon as the primary material used in field effect transistors. The real question currently, the one that this paper addresses, is whether using semiconductor graphene methods in field effect transistors will produce transistor performance results greater than, equal to, or less than those of using silicon.

Theory

With their discovery single-handedly kickstarting the Digital Revolution of the 20th century, transistors are one of the most influential inventions of the Information Age and form the basis of practically all modern electronics. Replacing the clunky vacuum tubes that made up the massive first-generation computers, the discovery of transistors allowed for a much smaller, more durable, and more efficient electrical switch [2]. Today, the most popular type of transistor being used in everything from computers to electric cars is the Field Effect Transistor (FET), making up around 99.9% of all transistors in everyday use [3]. As its name suggests, all FETs use electric fields to control or amplify an electric current based on the voltage that is given to them [4]. Generally, the physical structure of FETs is classified into three main layers of different materials: the substrate, the insulator, and the electrode. The substrate region, which is usually made of semiconductor silicon, makes up the lower main body of the transistor and provides the structure for the other regions to sit on. The substrate itself is also split up into two contrasting regions, namely n-type regions and p-type regions, further dividing the larger substrate into a smaller body and an electrical current channel. As the substrate is created, depending on whether n doping or p doping takes place, that corresponds to which type of FET it is, which region the electrical channel is, and oppositely corresponds to what region the body is. The layer located on top of the substrate and under the gate electrode is the insulator, which is usually made of silicon dioxide, and functions as a buffer between the two conductive regions above and below it. Without the insulator, the gate and substrate would be touching, causing the transistor to stop working altogether as it would be in a constant state of either always on or always off. The final layer are the electrodes, which are commonly made of highly conductive metals like platinum or rhodium, and function as electrical terminals where current flows throughout. A FET will commonly have at least these three basic electrodes: source and drain, which are both located on top of the substrate, and gate, which is located on top of the insulator. The way a transistor works is that the source and drain electrodes are connected to the electrical channel, and current flows from source to drain. By applying different voltages to the gate electrode, it controls the width of the channel and thus current conduction between the drain and source.

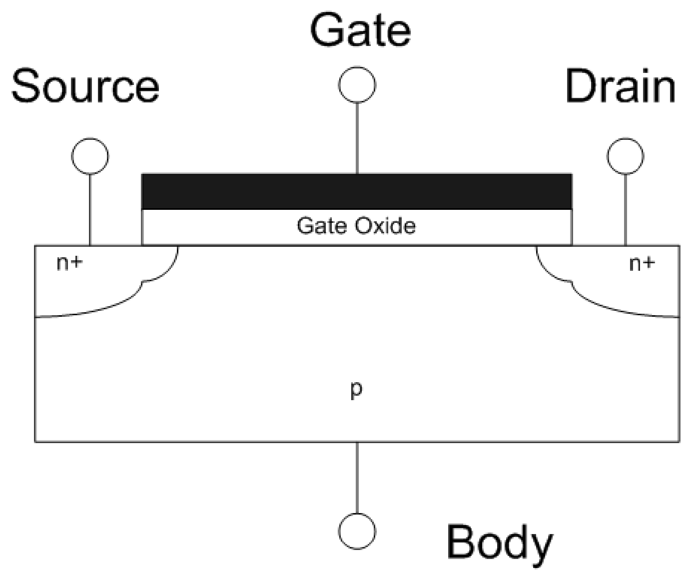

Figure 2. Basic component diagram of a field effect transistor

Determining the performance of a specific FET involves examining the data shown in IV graphs, also known as current vs voltage graphs. This type of graph plots how much current exits out of the drain terminal based on how much starting voltage is applied to the source terminal, for different values of gate voltage. If the current being conducted through the channel is a value that is higher than that of another transistor at the same voltages, then we can tell that the higher current transistor performs better and conducts more current through than the other one.

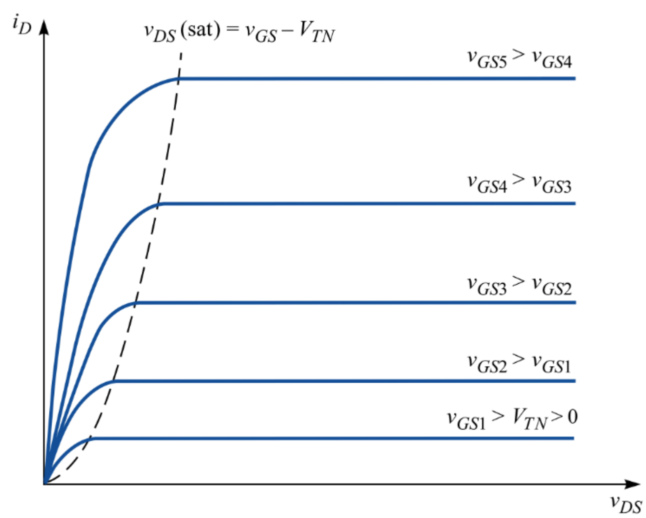

Figure 3. Voltage drops from source to drain (V) vs drain current (A) for an ideal FET at varying gate voltages [5]

This is the voltage vs current graph in the ideal case for an n type FET, and there are two main regions for each curve which are split by the Vds (sat), or the saturation voltage. The left side of the saturation voltage is called the triode region, and it's where voltage essentially has a linear relationship with current. In this region, as the voltage increases, so does the drain current, and it continues to do so until it reaches its maximum current capacity. At this point, the saturation region begins, and here the transistor can be thought of as carrying its full capacity of current. In this region, no matter how much additional voltage you apply, the drain current value will remain essentially constant. Although each of the curves displayed on the graph follow the same pattern, the difference between them is the amount of gate voltage applied. It is also worth noting that as the gate voltage goes up, the saturation voltage goes up with it, with the maximum current capacity exponentially rising.

Materials and Methods

The simulation software which will be used to determine transistor performance results is the Graphene Field Effect Transistor (GFET) tool on Nanohub.org. Nanohub.org is a science and engineering website which has community contributed simulation tools geared towards education, and this tool that will be utilized in this paper was provided by the University of Illinois Urbana Champaign. In the input data, there are options to change basic settings and advanced settings. Basic settings include values such as the width of the graphene, length of the graphene, voltage applied to the gate, thickness of the oxide on the top gate, electron mobility, and more. Advanced settings include data such as the thermal conductivity of graphene, thermal conductivity of the substrate, thermal conductivity of the insulator, and oxide thickness of the back gate. The output data are in the form of line graphs, including voltage vs current, temperature vs position, velocity vs position, electron density vs position, and hole density vs position. This paper will specifically focus on varying the width, length, electron mobility, and thermal conductivity values to see changes in the various properties, with the ultimate purpose of determining if the two methods for semiconducting graphene produce better or worse results than silicon in terms of transistor performance as demonstrated by the voltage vs current graph.

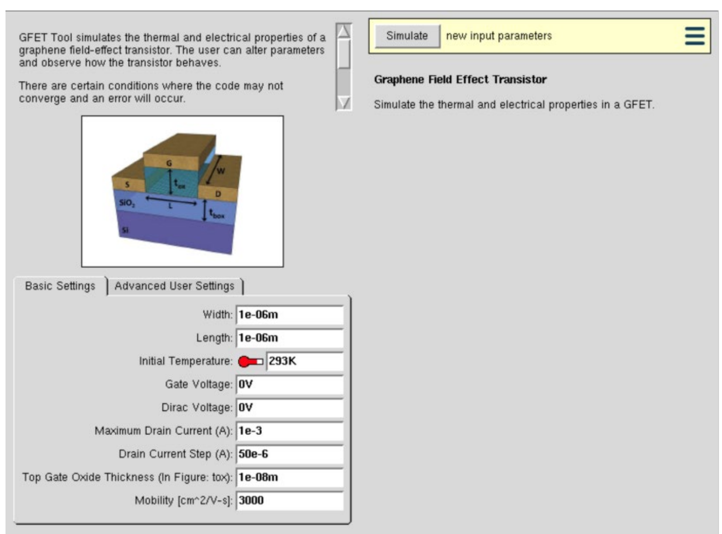

Figure 4. GFET tool provided by UIUC located on Nanohub.org.

Results

The following sections describe simulations with different input parameters and output graphs.

Preliminary Results

Prior to investigating the graphene FETs, we first established a baseline for comparison by simulating the results on pure silicon-based FETs. For this simulation of voltage vs current, we used prior research to assume that the electron mobility value is 307.2 cm^2/Vs [6], thermal conductivity is 4 W/mK [7], and all other values are at their default.

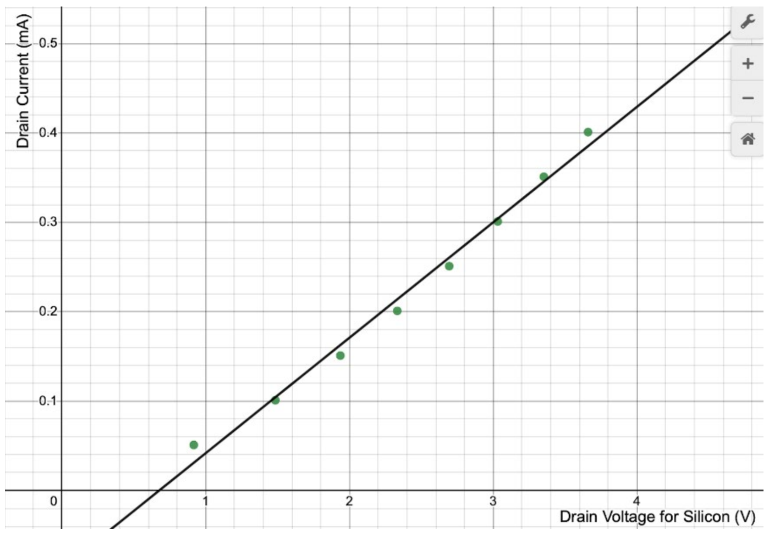

Figure 5. Drain voltage vs drain current for silicon

The graph indicates a positive linear relationship y = -0.087135 + 0.12911x between the drain voltage and drain current, with a correlation of r = 0.9948. The constant of determination r^2 for this curve is 0.9896, meaning that almost 99% of changes in drain current can be predicted by the changes in drain voltage. These results won't be discussed in depth, but they are included simply to provide a glimpse into how a traditional FET transistor may perform and to give a ground for comparison.

Reduced Graphene Oxide (rGO)

Reduced graphene oxide, or rGO for short, is a modified version of oxidized graphene, which comes from oxidizing graphite. Scientists have known about the composite graphite oxide for over a hundred seventy years now, but only quite recently has their potential use in electronics been a hot topic of research. Unlike pure graphene, graphene oxide is not only cheap and abundant [8], but also can be readily applied to many use cases such as solar cells, chemical sensors, and more [9]. Compared with the original supermaterial, reduced graphene oxide involves a modification that reduces the number of oxygen atoms bonded with the graphene, essentially morphing it back into a more pure form of graphene while still retaining the oxygen. There are two main ways of reducing graphene in a controlled amount, chemical reduction and thermal reduction [10]. Chemical reduction involves using hydrazine vapors to form a chemical reaction and get rid of some of the oxygen. Thermal reduction involves heating graphene oxide to high temperatures inside of an inert gas. Whichever method is used, as long as it is performed in moderation, results in a substantial opening of a band gap, turning the graphene into a semiconductor. Scientists do have to control the reduction, however, since reducing the oxygen too much will simply leave pure graphene, which has no band gap.

We then isolated and investigated the following four properties for a reduced graphene oxide based FET. For the purposes of consistency, assume that all of these measurements are based on a reduced graphene oxide sheet that has an electron mobility of 320 cm^2 / V*s and a thermal conductivity of 6300 W/mK.

Electron Mobility

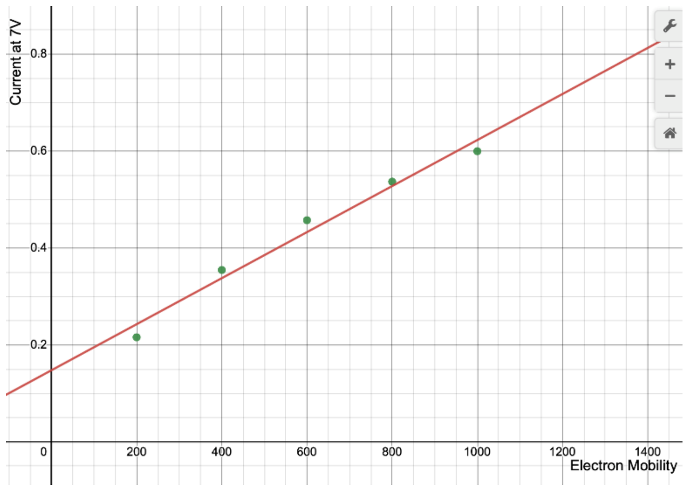

Figure 6. Electron mobility vs current at 7V for reduced graphene oxide

From this graph, based on table S1, it is evident that there is a direct relationship between the two variables. The graph can be approximated by the equation y = .14778 + .00047494x, which follows a linear fit and has a correlation of r = 0.9878.

Thermal Conductivity

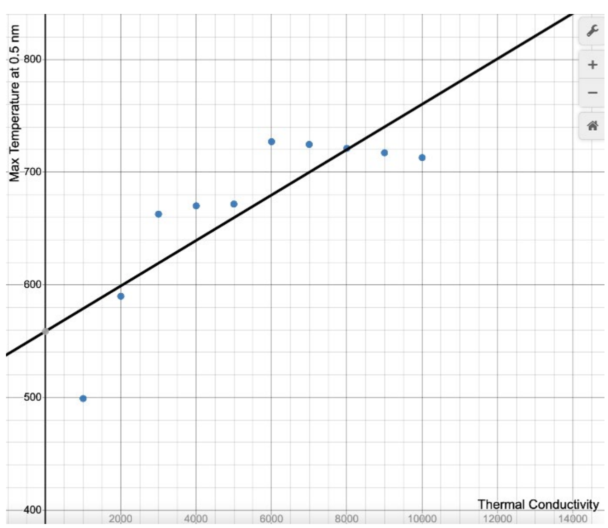

Figure 7. Thermal conductivity vs max temperature at 0.5nm position for reduced graphene oxide

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From this graph, based on table S2, it is evident that there is a direct relationship between the two variables, although it does not fit the data as well as most of the other graphs. The graph can be somewhat approximated by the equation y = 558.754 + 0.0201635x, which follows a linear fit and has a correlation of r = 0.8305.

Top Gate Oxide Thickness

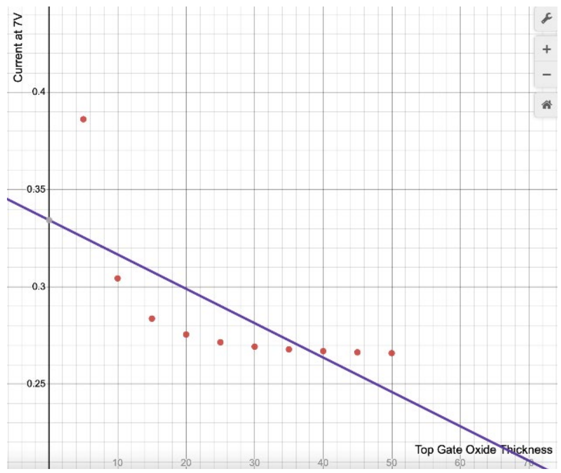

Figure 8. Top gate oxide thickness vs current at 7V for reduced graphene oxide

From this graph, based on table S3, it is evident that there is a direct negative relationship between the two variables, although, once again it does not fit the data as well as most of the other graphs. The graph can be somewhat approximated by the equation y = 0.334299 - 0.00176582x, which follows a linear fit and has a correlation of r = -0.7187.

Channel Length

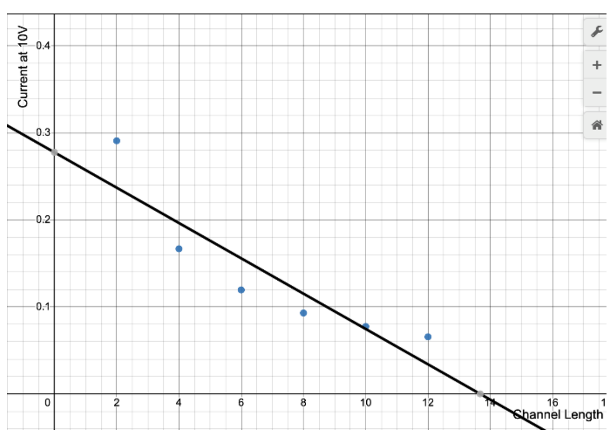

Figure 9. Channel length vs current at 10V for reduced graphene oxide

From this graph, based on table S4, it is evident that there is a direct negative relationship between the two variables. The graph can be approximated by the equation y = 0.277606 - 0.0202992x, which follows a linear fit and has a correlation of r = -0.902.

Doped Graphene

Doping, which is defined as introducing impurities into the graphene's band structure, is another viable method of turning graphene into a semiconductor. There are two major styles of graphene doping being applied: surface transfer doping and substitutional doping [11]. Surface transfer doping of graphene happens when dopants such as gold, bismuth, and antimony interchange electrons with the surface atoms of a sheet of graphene. Substitutional doping, a more traditional doping method, occurs when a carbon atom in the graphene lattice is replaced by an atom of the foreign dopant. Either of these methods, if done correctly, seems to work in creating a small but necessary bandgap, thus turning graphene into a semiconductor. It is important to note however, that doped graphene is not as simple to produce as graphene oxide or silicon. We then isolated and investigated the following four properties for a doped graphene-based FET. For the purposes of consistency, assume that all of these measurements are based on a doped graphene sheet that has an electron mobility of 550 cm^2 / V*s and a thermal conductivity of 4000 W/mK [12].

Electron Mobility

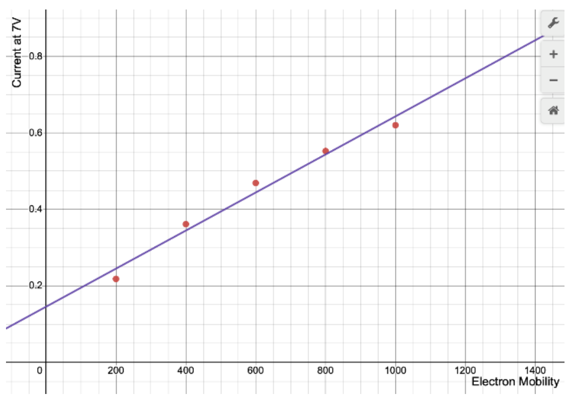

Figure 11. Electron mobility vs current at 7V voltage for doped graphene

From this graph, based on table S5, it is evident that there is a direct relationship between the two variables. The graph can be approximated by the equation y = 0.14557 + 0.000497873, which follows a positive linear fit and has a correlation of r = 0.9889.

Thermal Conductivity

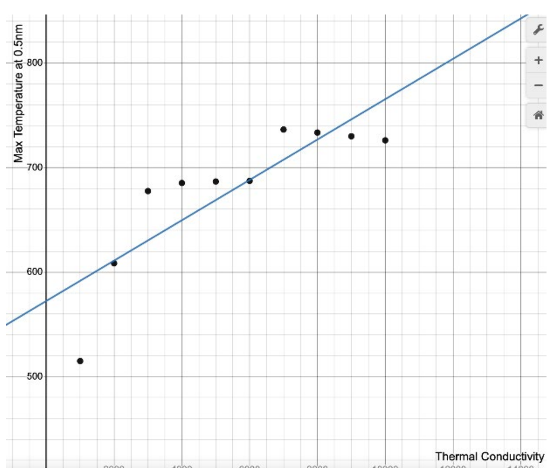

Figure 12. Thermal conductivity vs maximum temperature at 0.5 nm position for doped graphene.

From this graph, based on table S6, it is evident that there is a direct relationship between the two variables, although it does not fit the data as well as most of the other graphs. The graph can be somewhat approximated by the equation y = 572.387 + 0.0193022x, which follows a linear fit and has a correlation of r = 0.844.

Top Gate Oxide Thickness

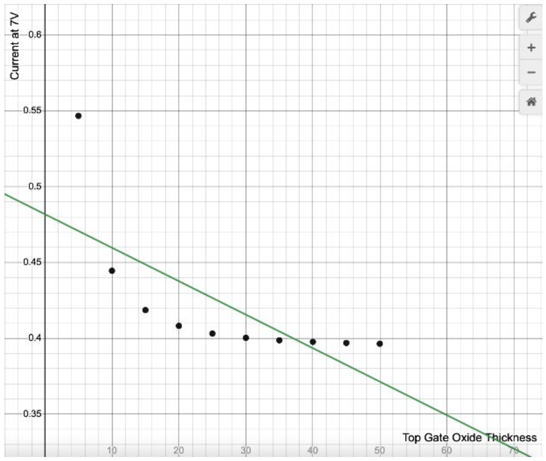

Figure 13. Top gate oxide thickness vs current at 7V for doped graphene

From this graph, based on table S7, it is evident that there is a direct negative relationship between the two variables, although, once again it does not fit the data as well as most of the other graphs. The graph can be somewhat approximated by the equation y = 0.481782 - 0.00220727x, which follows a linear fit and has a correlation of r = -0.7181.

Channel Length

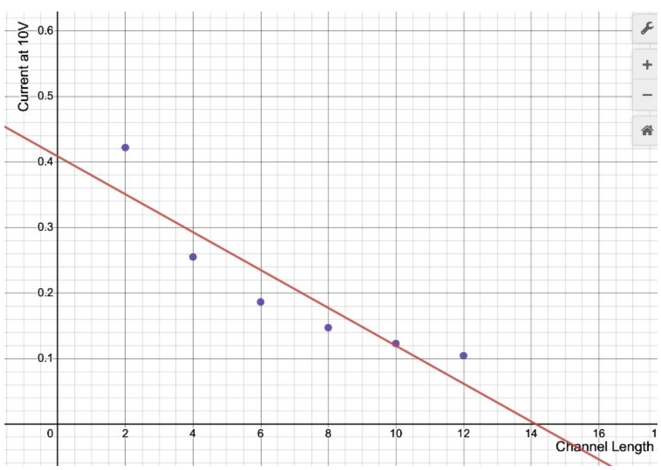

Figure 14. Channel length vs current at 10V for doped graphene

From this graph, based on table S8, it is evident that there is a direct negative relationship between the two variables. The graph can be approximated by the equation y = 0.408625 - 0.0289031x, which follows a linear fit and has a correlation of r = -0.9133.

4.4 Comparisons

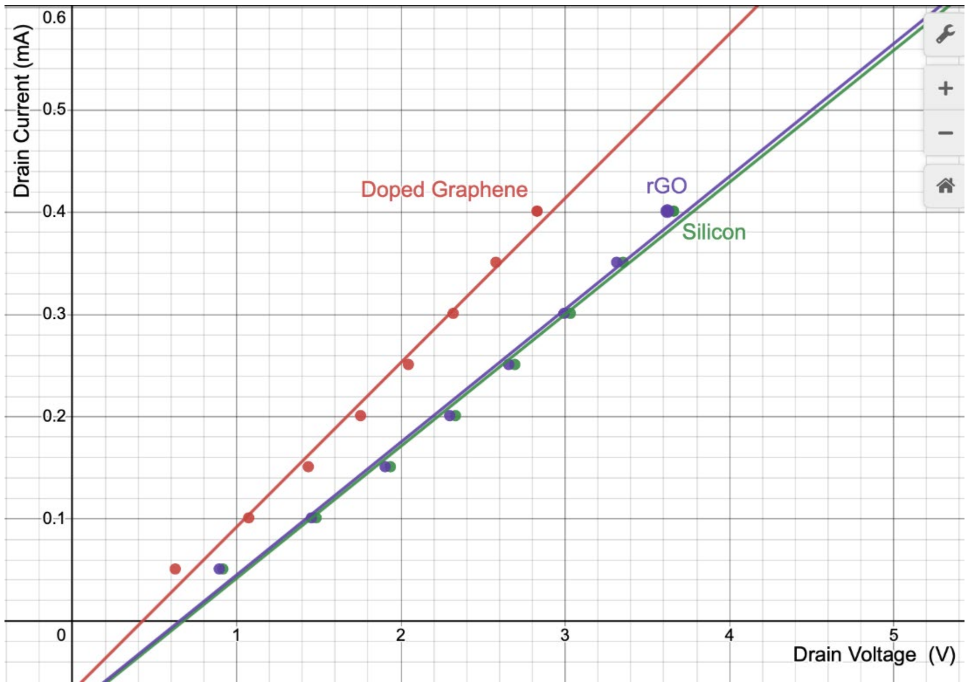

Figure 15. Comparisons between the drain voltage vs drain current graphs for doped graphene, reduced graphene oxide (rGO), and silicon.

This graph, based on Table S9, includes three different data sets and corresponding fit lines: one for doped graphene, which uses an electron mobility of 550 cm^2/Vs and a thermal conductivity of 4000 W/mK; one for reduced graphene oxide (rGO), which uses an electron mobility of 320 cm^2/Vs and a thermal conductivity of 6300 W/mK; and silicon, which uses an electron mobility of 307.2 cm^2/Vs and a thermal conductivity of 4 W/mK. For the silicon data set, the line of best fit equation was y = -0.087135 + 0.12911x, with a correlation of r = 0.9948. The constant of determination r^2 was 0.9896, so silicon's drain current can very accurately be predicted by the changes in drain voltage. For the doped graphene data set, the line of best fit equation was y = -0.06861 + 0.160778x, with a correlation of r = 0.9953. The constant of determination r^2 was 0.9906, so doped graphene's drain current can also very accurately be predicted by the changes in drain voltage. Finally, for the rGO data set, the line of best fit equation was y = -0.0868702 + 0.130682x, with a correlation of r = 0.9955. The constant of determination r^2 was 0.9911, so doped graphene's drain current can also very accurately be predicted by the changes in drain voltage.

Discussion and Conclusion

The two main issues that this essay addresses are firstly, concerns of whether graphene performs better, worse, or equal to silicon, and secondly, whether using graphene in FETs is a viable improvement to the transistor industry or not. Onto the first concern, as you can see from the comparisons graph, the red graph, doped graphene, outperformed the purple graph, rGO, which slightly outperformed the green graph, silicon. We know this because we see the red graph reach the same current at a lower voltage value, indicating that doped graphene is predicted to reach almost 0.5 mA of current at a similar voltage as the silicon which only reaches about 0.4 mA. This difference of 0.1 mA of current at ~3.6 V is quite significant of a difference, meaning that doped graphene-based transistors would make the transistor industry more efficient, should they be implemented widely. Since both options of graphene followed the exact same patterns for each of the properties, just with varying values. Which graphene option is truly the best? We conclude that the best option for silicon replacement is the reduced graphene oxide due to it by far being the most abundant and extensively studied form of graphene. While graphene is an exotic material that has many interesting properties, the main roadblock for widespread graphene implementation is indeed quantity, not quality [13]. In other words, graphene is a nearly complete package, and the only thing that is missing is production. While it may be beneficial in the future to consider switching to doped graphene if scientists find a way to mass produce it, now, reduced graphene oxide still outperforms silicon, is easier to produce, and has more research to back it up. With the already ubiquitous usage of transistors in our everyday lives, a switch to reduced graphene oxide-based transistors could bring revolutionary benefits for the electronics industry such as smarter cell phones, faster computers, and more accurate biosensors.

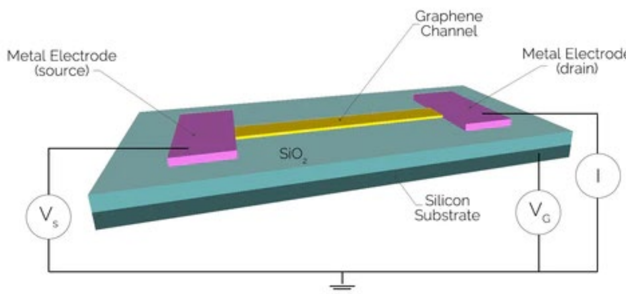

Figure 16. Diagram of a potential future graphene-based transistor.

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